Claims

1. A decoder apparatus comprising:

a likelihood estimator for generating a sequence of bit value likelihood estimates of a sequence of bit values of multi bit symbols of a data sequence;

a first decoder element for generating a first decoded data sequence in response to the bit value likelihood estimates;

a weighting processor for generating a weighted compensation data sequence in response to the first decoded data sequence and reliabilities of the data of the first decoded data sequence;

and wherein the likelihood estimator is operable to modify the sequence of bit value likelihood estimates in response to the weighted compensation data.

2. A decoder apparatus as claimed in claim 1 wherein the first decoder element is a Maximum A Posteriori (MAP) decoder.

3. A decoder apparatus as claimed in claim 1 wherein the first decoder element is a Soft Output Viterbi Algorithm (SOVA) decoder

4. A decoder apparatus as claimed in any of the claims 1 to 3 wherein the first decoded data sequence comprises data values associated with the reliabilities of the data of the first decoded data sequence.

5. A decoder apparatus as claimed in any of the claims 1 to 4 wherein the data sequence comprises an uncoded information data sequence, a first coded sequence generated from encoding of data of the information data sequence and a second coded sequence generated from encoding of interleaved data of the information data sequence;

wherein the first decoder is operable to generate the first decoded sequence in response to bit value likelihood estimates of the information data sequence and the first coded sequence;

the decoder apparatus further comprising:

an interleaver coupled to the output of the first decoder element;

a second decoder element coupled to the interleaver and operable to generate a second decoded data sequence in response to bit value likelihood estimates of the information sequence and the second coded sequence.

6. A decoder apparatus as claimed in claim 5 wherein the second decoder element is a Maximum A Posteriori (MAP) decoder.

7. A decoder apparatus as claimed in claim 5 wherein the second decoder element is a Soft Output Viterbi Algorithm (SOVA) decoder.

8. A decoder apparatus as claimed in claim 5 to 7 wherein the second decoder is operable to further generate the second decoded data sequence in response to the first decoded data sequence.

9. A decoder apparatus as claimed in any of the claims 5 to 8 wherein the decoder apparatus further comprises a de-interleaver coupled between the output of the second decoder element and the input of the first decoder element and wherein the first decoder element is operable to further generate the first decoded data sequence in response to the second decoded data sequence.

10. A decoder apparatus as claimed in claim 9 wherein the decoder apparatus is a turbo decoder apparatus.

11. A decoder apparatus as claimed in any of the claims 5 to 10 wherein the weighting processor is operable to generate weighted compensation data for the information data sequence in response to the first decoded data sequence and reliabilities of the data of the first decoded data sequence.

12. A decoder apparatus as claimed in any of the claims 5 to 11 wherein the weighting processor is operable to generate weighted compensation data for the first coded data sequence in response to the first decoded data sequence and reliabilities of the data of the first decoded data sequence.

13. A decoder apparatus as claimed in claim 12 wherein the first decoded data sequence comprises decoded data corresponding to the first coded data sequence.

14. A decoder apparatus as claimed in any of the claims 5 to 13 wherein the weighting processor is operable to generate weighted compensation data for the information data sequence in response to the second decoded data sequence and reliabilities of the data of the second decoded data sequence.

15. A decoder apparatus as claimed in any of the claims 5 to 14 wherein the weighting processor is operable to generate weighted compensation data for the second coded data sequence in response to the second decoded data sequence and reliabilities of the data of the second decoded data sequence.

16. A decoder apparatus as claimed in claim 15 wherein the second decoded data sequence comprises decoded data corresponding to the second coded data sequence.

17. A decoder apparatus as claimed in any of the claims 5 to 16 wherein the second decoded data sequence comprises data values associated with the reliabilities of the data of the second decoded data sequence.

18. A decoder apparatus as claimed in any of the previous claims wherein the decoder apparatus is operable to iterate the decoding operation.

19. A decoder apparatus as claimed in any of the previous claims wherein the weighting processor is operable to weight each bit of the weighted compensation data in response to the likelihood of that bit being a given value.

20. A decoder apparatus as claimed in claim 19 wherein the likelihood estimator is operable to modify a bit value likelihood estimate of a bit of the sequence of bit values in response to the weighted compensation data.

21. A decoder apparatus as claimed in any of the previous claims wherein the weighting processor is operable to set a value of a bit of the weighted compensation data sequence to a hard decision bit value if the reliability of the decoded data corresponding to the bit is above a threshold.

22. A decoder apparatus as claimed in any of the previous claims wherein the weighting processor is operable to set a value of a bit of the weighted compensation data sequence to a null value if the reliability of the decoded data corresponding to the bit is less than a threshold.

23. A decoder apparatus as claimed in claim 22 wherein the likelihood processor is operable not to modify a bit value likelihood estimate for a bit corresponding to a bit of the weighted compensation value having a null value.

24. A decoder apparatus as claimed in any of the previous claims wherein the bit value likelihood estimates are logarithmic likelihood ratios between the probability of a bit having a first value and a second value.

25. A decoder apparatus as claimed in any of the previous claims wherein the multi bit symbols comprise Quadrature Amplitude Modulated (QAM) symbols having more than four constellation points.

26. A decoder apparatus as claimed in any of the previous claims wherein the multi bit symbols comprises Phase Shift Keying (PSK) symbols having more than four constellation points

27. A subscriber unit for a 3rd Generation cellular communication system comprising a decoder apparatus according to any of the previous claims.

28. A 3rd Generation cellular communication system comprising a subscriber unit according to claim 27.

29. A method of decoding comprising repeating the steps of:

generating a sequence of bit value likelihood estimates of a sequence of bit values of multi bit symbols of a data sequence;

generating a first decoded data sequence in response to the bit value likelihood estimates;

generating a weighted compensation data sequence in response to the first decoded data sequence and reliabilities of the data of the first decoded data sequence; and

modifying the sequence of bit value likelihood estimates in response to the weighted compensation data.

30. A computer program enabling the carrying out of a method according to claim 29.